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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,413	11/10/2003	Hiroyuki Morishita	82478-1800	5180

21611 7590 02/21/2006

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EXAMINER	
PEERS, CHASE W	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,413	MORISHITA ET AL.	
	Examiner	Art Unit	
	Chase Peers	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

Claims 1-3 and 14-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy ("The Cache Memory book") and further in view of Suh et al. ("Dynamic Cache Partitioning for Simultaneous Multithreading Systems").

1. Regarding claims 1, and 14-16, Handy shows that a computer with a cache, main memory, a microprocessor, an address receiving unit, a caching unit to acquire the data block from main memory (pg 12, 51, and 52), having the address converting unit convert the logical address to the physical address, sending the address to the receiving unit, and storing the physical address in the cache were well known in the art (pg 12 and 52).

Furthermore, Handy further shows an address receiving unit to receive a logical address, a data block managing unit to manage data stored in the cah using the logical addresses, and an address converting unit to convert the address to the physical address and sent it to main memory (pg 12 and 52). However, Handy does not expressly show a region-managing unit to manage regions in the cache.

Suh et al. does teach the use of a region-managing unit that manages regions in cache.

Handy and Suh et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow for dynamic partitioning. The suggestion for doing so would have been to increase cache performance. Therefore, it would have

been obvious to combine Suh et al. and Handy for the benefit of a more efficient cache to obtain the invention as specified in claims 1 and 14-16.

2. Regarding claims 2 and 3, Suh et al. goes on to further describe that the region managing unit divides the cache into a plurality of regions equal to the number of tasks and finds out how many tasks are running and divides the cache based on the information.

Handy and Suh et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to allow for these features of dynamic partitioning. The suggestion for doing so would have been to increase cache performance. Therefore, it would have been obvious to combine Suh et al. and Handy for the benefit of a more efficient cache to obtain the invention as specified in claims 1 and 14-16.

Claims 4 and 7-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy and Suh et al. as applied to claims 1-3 above, and further in view of Patterson et al ().

3. Regarding claim 4, Handy and Suh et al. described all of the limitations of claims 1-3 and Suh et al. further describes having the region management unit managing a plurality of regions in a one-to-one correspondence with task (process) identifiers. Neither Handy nor Suh et al. expressly describe a task identifier unit to receive task identifiers or a caching unit that stores acquired data blocks in the cache corresponding to the received task identifier.

Patterson et al. does describe a task identifier unit to receive task identifiers or a caching unit that stores acquired data blocks in the cache corresponding to the received task identifier.

Handy, Suh et al. and Patterson et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to attach task identifiers to data in the cache. The suggestion for doing so would have been correctly separate and earmark data. Therefore, it would have been obvious to combine Patterson et al., Suh et al. and Handy for the benefit of classification to obtain the invention as specified in claim 4.

4. Regarding claim 7, Patterson et al. shows that the task identifier could be a process identifier assigned and ran by the operating system (pg 598) and evidentiary support shows that a microprocessor that could perform multitasking under the control of an operating system for a while (Review of operating systems).

Handy, Suh et al. and Patterson et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to attach task identifiers to data in the cache. The suggestion for doing so would have been correctly separate and earmark data. Therefore, it would have been obvious to combine Patterson et al., Suh et al. and Handy for the benefit of classification to obtain the invention as specified in claim 7.

5. Regarding claims 8-11, Patterson et al. shows that a judging unit operable to judge if data is stored in the cache by searching all regions (i.e. a hit check), a judging unit operable to judge if data is stored in the cache by searching a region corresponding to the task (i.e. an associative hit check), a cache made up of a plurality of ways where regions each contain at least one way and a set associative mapping for each region containing more than one way (i.e. a set associative cache) are all well known in the art (pgs. 13, 14, 51, and 54).

Handy, Suh et al. and Patterson et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to attach task identifiers to data in the cache. The suggestion for doing so would have been correctly separate and earmark data. Therefore, it would have been obvious to combine Patterson et al., Suh et al. and Handy for the benefit of classification to obtain the invention as specified in claims 4 and 8-11.

Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, Suh et al. and Patterson et al. as applied to claims 1-4 above, and further in view of Thaler et al. (Pat No 5983329).

6. Handy, Suh et al. and Patterson et al. describe all the limitations given in claims 1-4, but do not expressly disclose the task identifier being an address of the data location in main memory.

Thaler et al. does describe the task identifier being the address of the data location in main memory (column 4, lines 38-46).

Handy, Suh et al., Patterson et al. and Thaler et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the task identifier be the address of the data in main memory. The suggestion for doing so would have been to save cache space while still uniquely identifying all data in the cache. Therefore, it would have been obvious to combine Handy, Suh et al., Patterson et al. and Thaler et al. for the benefit of saved space to obtain the invention as specified in claim 5.

Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, Suh et al. and Paterson et al. as applied to claims 1-4 above, and further in view of Hum et al. (Pub No 20020087824).

7. Handy, Suh et al. and Patterson et al. describe all the limitations given in claims 1-4, but do not expressly disclose that the task identifier is generated by converting an address of a location in the main memory at which the task is stored as a program.

Hum et al. does disclose the task identifier is generated by converting an address of a location in the main memory at which the task is stored as a program (paragraph 16).

Handy, Suh et al., Patterson et al. and Hum et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention

it would have been obvious to a person of ordinary skill in the art to have the task identifier be a derivation of the address of the data in main memory. The suggestion for doing so would have been to have a unique identifier for each set of data in the cache while still being able to extract the address of the data in main memory and thus saving space. Therefore, it would have been obvious to combine Handy, Suh et al., Patterson et al. and Hum et al. for the benefit of space saving to obtain the invention as specified in claim 6.

Claims 12 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, Suh et al. and Paterson et al. as applied to claims 1-4 above, and further in view of Chiou et al.

8. Regarding claims 12 and 13, Handy and Suh et al. describe all the limitations of claim 1, but do not expressly describe the limitations given in claims 12 and 13.

Chiou et al. disclose a region management unit that divides the cache into specific regions and nonspecific regions, manages the specific regions in correspondence w/ a specific task where the caching unit stores the acquired data into the specific region if the task is a specific task, a microprocessor that executes tasks where a region management unit divides the cache into two regions, the first region holds a first and second task while a second region holds a third task, and the caching unit stores the acquired data blocks into the region in cache that they are supposed to go.

Handy, Suh et al., Paterson et al. and Chiou et al. are analogous art because they are from a similar problem solving area, cache memory. At the time of the invention

it would have been obvious to a person of ordinary skill in the art to divide up the cache into multiple regions. The suggestion for doing so would have been to correctly separate data. Therefore, it would have been obvious to combine Handy, Suh et al., Paterson et al. and Chiou et a. for the benefit of a more efficient cache to obtain the invention as specified in claims 12 and 13.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. A copy of the cache entry from Wikipedia to show that many of the claims are well known in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chase Peers whose telephone number is (571) 272-6757. The examiner can normally be reached on from Monday to Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
2/15/06